Example of a Risk Information Sheet

<table>
<tr><td>ID TS 001</td><td colspan="2">Risk Title Chemistry DRAM</td><td>Identified 4/19/99</td></tr>
<tr><td>Priority</td><td colspan="3" rowspan="3">Statement
Since there are a limited number of DRAM spares between the Aqua and Aura spacecraft and Aqua is given first priority; there may be inadequate DRAM to meet the two-orbit data storage requirements for the Aura Solid State Recorder (SSR).</td></tr>
<tr><td>Probability
Medium</td></tr>
<tr><td>Impact
High</td></tr>
<tr><td>Timeframe
Near Term</td><td>Submitter Name
Andrea Razzaghi</td><td>Class</td><td>Assigned to
Andrea Razzaghi</td></tr>
<tr><td colspan="4">Context
TRW plans to meet the current two-orbit data storage requirements by augmenting the DRAM units reserved for Chemistry with DRAM units currently being reserved as PM spares. There are no more DRAM units available beyond those currently allocated for PM and Chemistry. The Common Bus SSR design is based on these 5.4V DRAM units (current technology is 3V).</td></tr>
<tr><td colspan="4">Mitigation Strategy
A. Track the Usage and Attrition of DRAM
B. Enable OMI Data Compression
C. Challenge Data Storage Requirements
D. Redesign SSR</td></tr>
<tr><td colspan="4">Contingency Plan and Trigger
· Spacecraft trigger point for using mitigation B is when the amount of DRAM available for the Chemistry SSR is less than the amount required to meet the two-orbit data storage requirements without OMI data compression implemented (less than 104 Gbits). IAM trigger point is TBD. Ground system trigger point is TBS.
· Spacecraft trigger point for using mitigation strategy C is when the amount of DRAM available for the Chemistry SSR is less than the amount required to meet the two-orbit data storage requirements with OMI data compression implemented (100 Gbits).
· TRW indicates that there would be an impact to the launch date for using mitigation strategy D due to the immaturity (not flight qualified) or the alternative high-density technology.</td></tr>
</table>

Status **Status Date** 11-2-99

Results of electrical testing indicated that 127 of 128 of the recovered DRAM stacks are acceptable for flight. TRW completed removal of DRAM units from eight remaining damaged boards and in the process dropped 64 DRAM units upon removal from one of the boards. The capability to trace SSR failures to the particular DRAM unit has been verified. The SSR has diagnostic telemetry to identify any failed device and determine the physical as well as logical address. Further, TRW does not plan on mixing the recovered parts and virgin parts on the same board, so that any failures can easily be traced to recovered parts. Some recovered DRAM stacks have shown evidence of solder voids. The core memory board de-laminated. Problem appears to be due to skipping bakeout prior to vapor-phase soldering. DRAM was successfully removed. TRW removed the Chemistry Solid State Recorder from the weekly "Top 10" List once at least 3 PM memory boards populated with recovered DRAM had successfully passed electrical testing. Since the test results were better than those with "virgin" DRAM, TRW no longer views use of recovered DRAM as a risk issue. TRW also found an additional 45 DRAM stacks in house and has reserved them for Chemistry, improving the situation further. Of those, the EOS program has received 16. They were subjected to a 100-hour burn-in at 125C at 110% voltage as a part of the lot qualification for EOS (i.e., these devices are flight units with 1000 hours of burn-in). The last PM memory board has competed trouble-shooting. There are 36 additional DRAM stacks requiring major rework that could be made available if successfully reworked.

PM SSR Status

The PM SSR Sub-unit mechanical integration is complete. Two DRAM stacks were replaced on one of the memory boards. Electrical integration and functional testing incomplete with some bit errors that are currently under investigation. Pre-conformal coat thermal cycling complete. Unit now in conformal coat process.

Approval	**Closing Date**	**Closing Rationale**